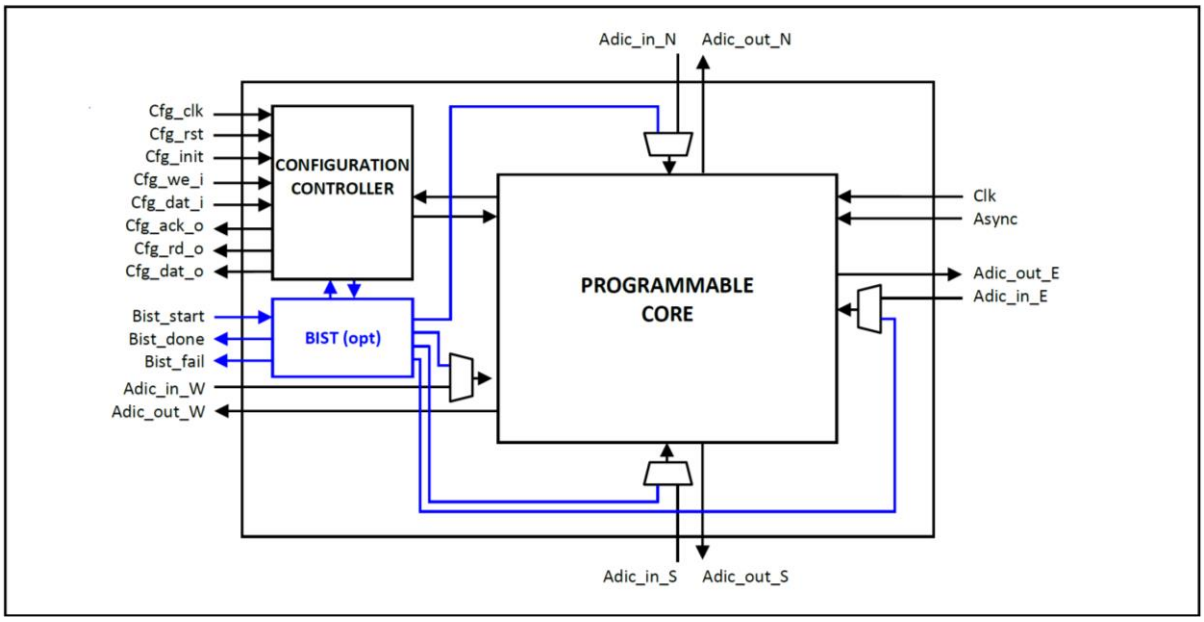


SPC Block Diagram

Overview

SPC (Synthesizable Programmable Core) is a soft FPGA core that is fully integrated into standard design flows and that allows the seamless implementation of generic RTL programmable logic in ASICs and SOCs.

The IP contains three modules:

- A Look Up Table (LUT) based programmable core, or FPGA, suitable for mapping generic RTL functions.
- A configuration controller for the interaction between SOC and FPGA system functions such as the loading/checking of the bitstream.
- A Built-In Self-Test for industrial grade manufacturing testing or in-system self-testing.

Product Features

Configuration

- Control interface.
- On the fly bitstream decompression and decryption.
- High granularity partial reconfiguration.

Test

- ATPG compatibility.
- BIST engine.
- Test vectors for manufacturing.
- Alpha scrubbing.
- CRC/ECC

Compilation Tool

- RTL to bitstream synthesis.
- Effort and/or Timing driven place and route.
- TCL shell for flexible use and integration into 3rd party software.

Business Model

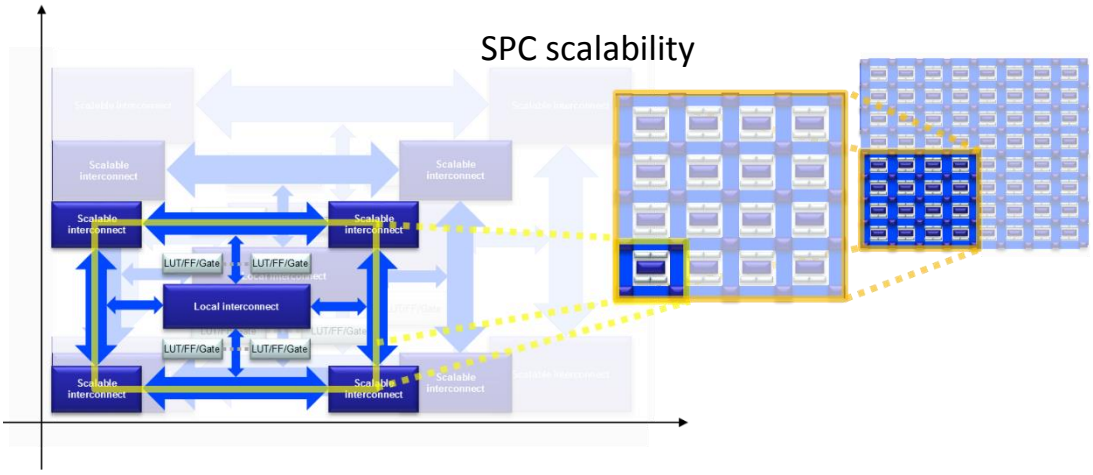
Access to the IP and corresponding compilation software is granted through a one-time license fee.
Adicsys offers optional annual support extensions: IP upgrades, software upgrades.
Software sub-licensing is possible through redistribution licenses.

SPC utilization examples

- Custom FPGA at a fraction of the cost and complexity of full-custom based approaches.
- Upgrade/Customization of several generations of products with a single ASIC.
- Test chips and Prototypes, early engineering samples.
- Analog ASSP's with reprogrammable on-chip FPGA.
- Integration of "companion FPGAs" to reduce bills of material.
- Debug and observation functions, On-Chip Logic Analyzer.
- Hidden functions, sensitive or confidential algorithms, non-permanent test logic.
- Customization and acceleration of processing units through upgradable instructions.
- Programmable Finite State Machines.
- Flexible chip interfaces.
- Encryption, data (pre)processing.

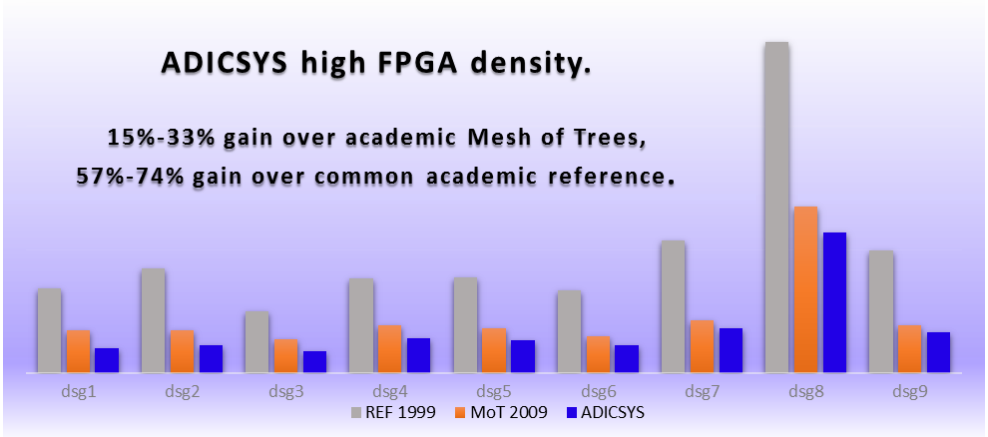
SPC disruptive soft FPGA technology

- Proprietary FPGA architecture that does not rely on full custom circuit design.
- Proprietary FPGA compilation software: customizable, distributable, no external licenses.
- 100% scalable and abuttable blocks.
- 50% configuration bits when compared to existing FPGA cores.
- Flexible configuration technology, improved reliability and SEU susceptibility over SRAM.
- Flexible bitstream compression directly supported by configuration controller.
- Virtually unlimited clock domains and flexible clock regioning.
- Virtually unlimited input/output ports.
- High granularity for partial reconfiguration.
- 90%+ resource usage.
- Technology independent IP, suitable for commercial/military/space applications and a full range of operating ranges from 180nm down to 14nm.



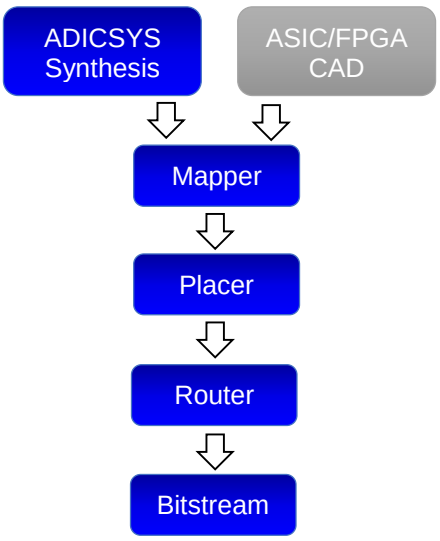
ADICSYS FPGA size

- Hundreds of LUTs to ten thousands LUTs per mm2 from 180nm to 14nm.
- IP cuts from 100 LUTs to 100k LUTs.
- SPC density tracks technology node feature size.
- Single or multiple SPC cores per chip.
- Multiple and flexible engagement models, e.g.:
  - 1% to 10% embedded FPGA area for localized programmable features.
  - 50% embedded FPGA area for custom programmable SOCs/FPGAs.



ADICSYS FPGA compilation suite

- ADICSYS distributable RTL front end:
  - Syntax checker
  - Elaboration
  - Synthesis
- Compilation suite accepts third party front ends for extended HDL language support.
- Compilation suite accepts third party synthesis (external licenses):
  - ASIC synthesis
  - FPGA synthesis
  - Special RTL generation (math, C++, …)
- ADICSYS technology mapper.
- ADICSYS effort driven FPGA Placer & Router.
- 100% compliant TCL shell.
  - Embeddable into top level Software
  - Easy and efficient scripting of custom FPGA compilation scenario



Synthesizable Programmable Core

ADICSYS

Benefits

- Fully integrated into RTL SOC design flow:
  - SPC IP RTL/gate simulation.
  - Accurate Timing Analysis.
  - No black box (LEF/GDSII).
  - No verification gap.
- Highly scalable and customizable:
  - Pre-existing SPC blocks
  - or
  - Custom size SPC blocks.
  - 100 to 100k LUTs.
  - Multiple SPC's per chip.
  - SPC LUT count is defined with single digit precision to optimize area.
- Technology independent:
  - Any CMOS node with digital capacity:
    - CMOS 180nm – 14nm
    - SOI
    - Rad-Hard
  - Any foundry.
  - Days/Weeks to deliver.
- No FPGA background required.
- One-time fee to use compilation tools.
- Independent FPGA technology:
  - SPC does not copy proprietary commercial FPGA structures (Logic Elements, LUTs, BitRAMs, DSPs …).
  - SPC does not rely on commercial FPGA software or third party software, although it is possible to use them.
- ADICSYS' FPGA software:
  - Linux support for ASIC integration.
  - Distributable for Linux and Windows end users.
- Compilation Runtime, RTL to bitstream:
  - 10k Gates per minute.

Deliverables

- SPC IP comprising:
  - Synthesizable RTL.
  - Bitstream Loader.
  - BIST.
- Synthesis, simulation and STA scripts.
- Place and route scripts and manual.
- Possibility to deliver GDSII in parallel.
- Test patterns.
- ADICSYS FPGA compilation software:
  - RTL Parser.
  - Synthesis.
  - FPGA place & route.
  - FPGA bitstream generation.
  - Embeddable TCL control shell.
- Operating systems:
  - Linux starting with RHEL4.
  - Windows starting with XP.
- Documentation, Examples, Training.
- Early SOC definition support.
- General ASIC design assistance.
- SPC customization.
- Standalone FPGA design assistance.

About ADICSYS

ADICSYS is a fabless semiconductor company that stands at the crossroad of ASIC design and FPGA technology. The company is built on fifteen years of experience in custom FPGA and embedded FPGA integration in industrial projects as well as leading edge semi-conductor products.
SPC is present on customer silicon since 2012.

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